1. An equalizer, comprising:

a differential analog tapped delay line comprising a plurality of N series connected analog delay cells, wherein each cell includes a pair of differential inputs and a pair of differential outputs, and wherein the differential analog tapped delay line receives an input signal to be equalized;

wherein, the differential input pair of the nth cell is connected to the differential output pair of the (n-1)th cell such that current is mirrored from the output pair to the input pair to form N-1 differential taps;

N-1 differential input multiplying digital to analog converters (MDAC), one connected at its differential input at each differential tap, each MDAC multiplying an analog signal at its input by a digital weighting factor value to produce an output at a differential output; and

a differential slicer receiving a sum of the differential outputs from each of the MDACs and producing an equalized output.

2. The equalizer according to claim 1, wherein the delay of each of the delay cells comprises at least one delay selected from the group consisting of a delay of less than one symbol time of a signal being equalized, a delay of approximately one eighth of one symbol time of a signal being equalized, and a tunable delay.

3. The equalizer according to claim 1, wherein the equalizer has a finite impulse response.

4. The equalizer according to claim 1, wherein the quality factor (Q) of each of the delay elements is tunable.

5. The equalizer according to claim 1, further comprising a differential transconductor circuit coupled to the input of the first delay cell of the delay line.

6. The equalizer according to claim 1, further comprising a current mirror circuit serving as a termination to the output of the delay line.

7. The equalizer according to claim 1, wherein the digital weighting factor values are represented as thermometer coded digital values.

8. The equalizer according to claim 1, wherein at least one of the digital weighting factors is a negative value, and wherein the negative value is represented by one of represented by either a bit value of the digital weighting factor, or by a reversed connection between an the MDAC and the digital tap.

9. The equalizer according to claim 1, further comprising:

a power spectrum estimator receiving the input signal to be equalized, estimating the power spectrum thereof, and producing an error signal output; and

a digital weighting factor calculator receiving the error signal output from the power spectrum estimator and computing the digital weighting factor values therefrom.

10. The equalizer according to claim 9, wherein the power spectrum estimator comprises:

a pulse extraction logic circuit that compares a input signal with a delayed version of the input signal to produce an output signal containing extracted pulses;

an averaging circuit receiving the output pulse and producing therefrom an averaged signal representing the averaged value of the output signal;

a subtracter that subtracts a reference signal from the averaged signal to produce a difference signal; and

an absolute value circuit that converts the difference signal to the error signal by taking the absolute value of the difference signal.

11. The equalizer according to claim 10, wherein the reference signal comprises a random digital signal passed through a pulse extraction logic circuit and an averaging circuit.

12. The equalizer according to claim 10, wherein the power spectrum estimator estimates the power spectrum using pulse extraction logic circuits that extract pulses of at least one of: one, two and three different pulse widths.

13. The equalizer according to claim 9, wherein the averaging circuit comprises a low pass filter.

14. A power spectrum estimator, comprising:

a pulse extraction circuit that compares a digital input signal with a delayed version of the digital input signal to produce an output signal containing extracted pulses;

an averaging circuit receiving the output pulse and producing therefrom an averaged signal representing the averaged value of the output signal;

a subtracter that subtracts a reference signal from the averaged signal to produce a difference signal; and

an absolute value circuit that converts the difference signal to an error signal by taking the absolute value of the difference signal.

15. The power spectrum estimator according to claim 14, wherein the reference signal comprises a random digital signal passed through a pulse extraction circuit and an averaging circuit.

16. The power spectrum estimator according to claim 14, wherein the power spectrum estimator estimates the power spectrum using pulse extraction logic circuits that extract pulses of at least one of: one, two and three different pulse widths.

17. The power spectrum estimator according to claim 14, wherein the averaging circuit comprising a low pass filter.

18. The power spectrum estimator according to claim 14, further comprising a weighting value multiplier that multiplies a weighting factor by the difference signal before the difference signal is applied to the absolute value circuit.

19. A power spectrum estimator, comprising:

a pulse extraction circuit that compares a digital input signal with a first delayed version of the digital input signal to produce a first extracted pulse output signal containing extracted pulses of a first pulse width, and compares the digital input signal with a second delayed version of the digital input signal to produce a second extracted pulse output signal containing extracted pulses of a second pulse width;

a first averaging circuit receiving the first extracted pulse output and producing a first averaged value of the output signal to produce a first averaged signal;

a first subtracter that subtracts a first reference signal from the first averaged signal to produce a first difference signal;

a second averaging circuit receiving the second extracted pulse and producing a second averaged value of the output signal to produce a second averaged signal;

a second subtracter that subtracts a second reference signal from the second averaged signal to produce a second difference signal; and

an adder that adds the magnitude of the first difference signal to the magnitude of the second difference signal to produce an output error signal.

20. A power spectrum estimator according to claim 19, wherein:

the pulse extraction circuit compares the digital input signal with a third delayed version of the digital input signal to produce a third extracted pulse output signal containing extracted pulses of a third pulse width; and further comprising:

a third averaging circuit receiving the third extracted pulse and producing a third averaged value of the output signal to produce a third averaged signal;

a third subtracter that subtracts a third reference signal from the third averaged signal to produce a third difference signal; and

wherein the adder further adds the magnitude of the third error signal to the first and second error signals to produce the output error signal.

21. The power spectrum estimator according to claim 20, wherein at least one of the first, second and third reference signals comprises a random digital signal passed through a pulse extraction circuit and an averaging circuit.

22. The power spectrum estimator according to claim 20, wherein the second delayed version of the input signal is delayed by approximately twice the delay of the first delayed version of the input signal, and wherein the third delayed version of the input signal is delayed by approximately three times the delay of the first delayed version of the input signal.

23. The power spectrum estimator according to claim 20, wherein at least one of the first, second and third averaging circuits comprises a low pass filter.

24. The power spectrum estimator according to claim 20, further comprising at least one of the following:

a first weighting value multiplier that multiplies a first weighting factor by the first difference signal before the first difference signal is applied to the adder.

a second weighting value multiplier that multiplies a second weighting factor by the second difference signal before the second difference signal is applied to the adder; and

a third weighting value multiplier that multiplies a third weighting factor by the third difference signal before the third difference signal is applied to the adder.

25. The power spectrum estimator according to claim 19, further comprising a tapped delay line, and wherein the first and second delayed versions of the input signal are produced by passing the input signal through a tapped delay line and extracting the first and second delayed versions of the input signal from delay line taps.

26. The power spectrum estimator according to claim 25, further comprising one of a phase locked loop and a delay locked loop, that generates a delay correction signal that adjusts the delay of the first and second delayed versions of the input signal.

27. The power spectrum estimator according to claim 20, wherein the third delayed version of the input signal is produced by passing the input signal through the tapped delay line and extracting the third delayed version of the input signal from a delay line tap.

28. The power spectrum estimator according to claim 27, further comprising one of a phase locked loop and delay locked loop that generates a delay correction signal that adjusts the delay of the third delayed version of the input signal.

29. The power spectrum estimator according to claim 19, further comprising:

a finite impulse response filter having tap weight values; and

a tap weight calculator receiving the output error signal and converting the output error signal to adjust the tap weight values.

30. An apparatus that estimates power in a signal, comprising:

means for extracting pulses of a specified pulse width from the signal;

means, coupled to the extracting means, for filtering the extracted pulses to produce a filtered pulse signal; and

means, coupled to the filtering means, for subtracting the filtered pulse signal from a reference to produce a difference signal representing an estimate of power in the signal.

31. The apparatus according to claim 30, further comprising means, coupled to the subtracting means, for taking the absolute value of the difference signal to represent the estimate of power in the signal.

32. The apparatus according to claim 30, further comprising means for applying a weighting factor to the difference signal.

33. The apparatus according to claim 30, further comprising means for converting the estimate of power to a digital value.

34. An apparatus that estimates power in a signal, comprising:

means for extracting pulses of a plurality of specified pulse widths from the signal to produce a extracted pulses at each specified pulse width;

means, coupled to the extracting means, for filtering the extracted pulses of each specified pulse width to produce a plurality of filtered pulse signals;

means, coupled to the extracting means, for subtracting each of the filtered pulse signals from a corresponding reference to produce a plurality of difference signals; and

means, coupled to the extracting means, for adding each of the difference signals to produce a sum representing an estimate of power in the signal.

35. The apparatus according to claim 34, further comprising means for taking the absolute value of each of the difference signals prior to adding.

36. The apparatus according to claim 34, further comprising means for applying a weighting factor to each of the difference signals prior to the adding.

37. The apparatus according to claim 34, further comprising means for converting the estimate of power to a digital value.

38. The apparatus according to claim 34, further comprising means for applying a filter tap weight calculating algorithm to the estimate of power to calculate a filter tap weight value.

39. A power spectrum estimator, comprising:

a pulse extraction circuit that compares a digital input signal with a delayed version of the digital input signal to produce an output signal containing extracted pulses;

a counter circuit receiving the output pulse and producing therefrom a count over a time interval representing the averaged value of the output signal;

a subtracter that subtracts a reference count from the averaged signal to produce a difference signal.

40. The power spectrum estimator according to claim 39, wherein the reference signal comprises a random digital signal passed through a counter.

41. The power spectrum estimator according to claim 39, wherein the power spectrum estimator estimates the power spectrum using pulse extraction logic circuits that extract pulses of at least one of: one, two and three different pulse widths.

42. The power spectrum estimator according to claim 39, further comprising a weighting value multiplier that multiplies a weighting factor by the difference signal before the difference signal is applied to the absolute value circuit.